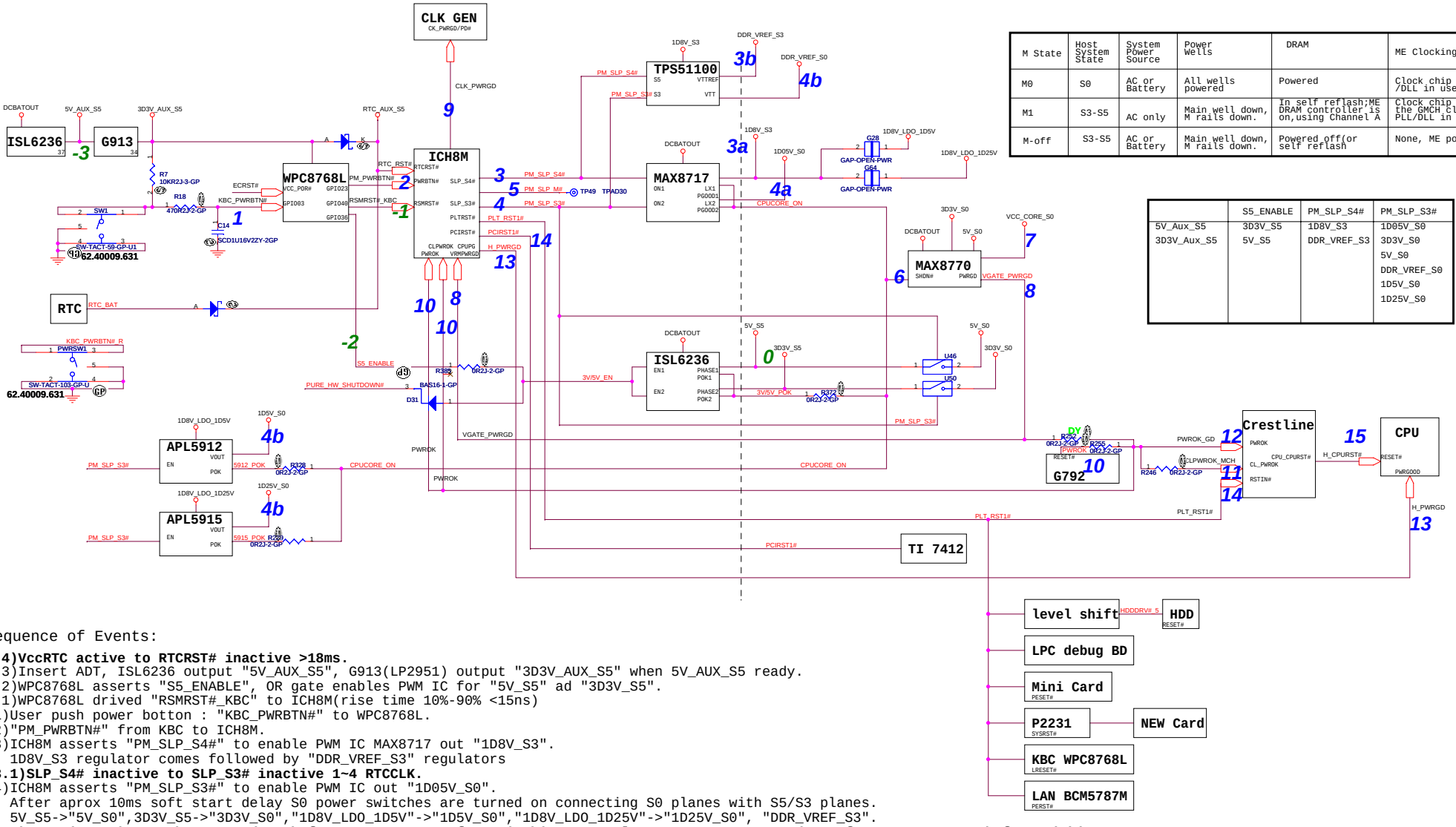
Biwa POWER TOPLOGY AND POWER SEQUENCING



M State	Host System State	System Power Source	Power Wells	DRAM	ME Clocking
M0	S0	AC or Battery	All wells powered	Powered	Clock chip powered and PLL /DLL in use.
M1	S3-S5	AC only	Main well down, M rails down.	In self reflash;ME DRAM controller is on,using Channel A	Clock chip powered with only the GMCH clock running and PLL/DLL in use.
M-off	S3-S5	AC or Battery	Main well down, M rails down.	Powered off(or self reflash	None, ME powered off.

	S5_ENABLE	PM_SLP_S4#	PM_SLP_S3#
5V_Aux_S5	3D3V_S5	1D8V_S3	1D05V_S0
3D3V_Aux_S5	5V_S5	DDR_VREF_S3	3D3V_S0
			5V_S0
			DDR_VREF_S0
			1D5V_S0
			1D25V_S0

Sequence of Events:

(-4)VccRTC active to RTCRST# inactive >18ms.
(-3)Insert ADT, ISL6236 output "5V_AUX_S5", G913(LP2951) output "3D3V_AUX_S5" when 5V_AUX_S5 ready.
(-2)WPC8768L asserts "S5_ENABLE", OR gate enables PWM IC for "5V_S5" ad "3D3V_S5".
(-1)WPC8768L drived "RSMRST#_KBC" to ICH8M(rise time 10%-90% <15ns)
(1)User push power botton : "KBC_PWRBTN#" to WPC8768L.
(2)"PM_PWRBTN#" from KBC to ICH8M.
(3)ICH8M asserts "PM_SLP_S4#" to enable PWM IC MAX8717 out "1D8V_S3".
1D8V_S3 regulator comes followed by "DDR_VREF_S3" regulators
(3.1)SLP_S4# inactive to SLP_S3# inactive 1~4 RTCCLK.
(4)ICH8M asserts "PM_SLP_S3#" to enable PWM IC out "1D05V_S0".
After aprox 10ms soft start delay S0 power switches are turned on connecting S0 planes with S5/S3 planes.
5V_S5->"5V_S0",3D3V_S5->"3D3V_S0","1D8V_LDO_1D5V"->"1D5V_S0","1D8V_LDO_1D25V"->"1D25V_S0", "DDR_VREF_S3".
(4.1)V5REF(5V_S0) must be powered up before 3D3V_S0, or after winthin 0.7V. Also V5REF must power down after 3D3V_S0, or before within 0.7V.
(4.2)1D5V_S0 must power up before V_CPU_IO(1D05V_S0) or after winthin 0.7V. Also V_CPU_IO must power down before 1D5V_S0 or after within 0.7V.
(5)PM_SLP_M# : TP.
(6)When 3V, 5V, 1.8V, 1.05V ready, they are asserts "CPUCORE_ON" to PWM IC for CPU power.
(7)5ms after VCC_CORE_S0 regulation, VGATE_PWRGD is driven to ICH8M VRMPWRGD.
(8)"G792_PWROK" Output remains low while VCC is below the reset threshold,
and for 220ms after VCC rises above the reset threshold.
(9)10ms after "VGATE_PWRGD" plane comes up "CLK_PWRGD" is driven.
(10)Power OK for ICH8M(PWROK assertion indicates that PCICLK has been stable for at least 1ms, Vcc supplies active to PWROK >99ms) .
(10.1)VGATE_PWRGD active to PWROK active >3 ms.
(11)CL_PWROK
(12)POWER OK for GMCH
(13)"H_PWRGD" from ICH8M to CPU
(14)"PLT_RST1#"(PCIRST1#) from ICH8M to GMCH.
(14.1)PWROK active to PLTRST1# active 34~41 RTCCLK
(15)"H_CPURST#" from GMCH to CPU

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